IN THE CLAIMS

1. (Original) A flash memory device comprising:

an array of addressable memory cells arranged in addressable blocks, the addressable blocks comprise a boot block and at least one additional memory cell block;

a first address decoder circuit coupled to the boot block;

a first voltage pump circuit coupled to the first address decoder circuit for providing a word line voltage signal to the boot block;

a second address decoder circuit coupled to the additional memory cell block; and

a second voltage pump circuit coupled to the second address decoder circuit for providing a word line voltage signal to the additional memory cell block.

2. (Original) The flash memory device of claim 1, wherein the first voltage pump circuit provides the word line voltage to the first address decoder circuit within a first time period, and the second voltage pump circuit provides the word line voltage to the second address decoder circuit within a second time period which is greater than the first time period.

3. (Original) The flash memory device of claim 1, wherein the first time period is less than about 300 nanoseconds.

4. (Original) The flash memory device of claim 1, wherein the second time period is less than about 2000 nanoseconds.

5. (Original) The flash memory device of claim 1, wherein the first and second voltage pump circuits generate a word line voltage of approximately five volts from a voltage supply of approximately three volts.

6. (Original) The flash memory device of claim 1, wherein the first voltage pump includes a first power supply connection, and wherein the second voltage pump includes a second power supply connection.

7. (Original) The flash memory device of claim 6, wherein the first power supply connection and the second power supply connection are each adapted to receive a power supply voltage.

8. (Original) The flash memory device of claim 7, wherein the first voltage pump is adapted to generate a first voltage greater than the power supply voltage.

9. (Original) The flash memory device of claim 8, wherein the second voltage pump is adapted to generate a second voltage greater than the power supply voltage.

10. (Original) The flash memory device of claim 1, wherein the first voltage pump includes a first deep power down mode that is not fully powered down.

11. (Original) The flash memory device of claim 10, wherein the second voltage pump includes a second deep power down mode that is not fully powered down.

12. (Original) The flash memory device of claim 11, wherein the first deep power down mode and the second deep power down mode are controlled by a reset/power-down signal.

13. (Original) The flash memory device of claim 1, wherein the second voltage pump is smaller than the first voltage pump.

14. (Original) The flash memory device of claim 1, wherein data stored in the boot block can be provided on an output data connection within approximately 300 ns following activation of the flash memory device.

15. (Original) The flash memory device of claim 1, wherein data stored in the additional memory cell block can be provided on the output data connection after the data stored in the boot block, and within approximately 2000 ns following activation of the flash memory device.

16. (Original) A processing system comprising:

a processor device; and

a flash memory device coupled to the processor device via at least address and data buses, the flash memory device comprising,

an array of addressable memory cells arranged in addressable blocks, the addressable blocks comprise a boot block and at least one additional memory cell block;

a first address decoder circuit coupled to the boot block;

a first voltage pump circuit coupled to the first address decoder circuit for providing a word line voltage signal to the boot block;

a second address decoder circuit coupled to the additional memory cell block; and

a second voltage pump circuit coupled to the second address decoder circuit for providing a word line voltage signal to the additional memory cell block.

17. (Original) The processing system of claim 16, wherein the flash memory device provides data on the data bus from the boot block within a first predetermined time period following activation of the flash memory device, and provides data stored in the additional memory cell block within a second predetermined time period which is greater than the first predetermined time period.

18. (Original) The processing system of claim 17, wherein the first time period is less then about 300 nanoseconds.

19. (Original) The processing system of claim 17, wherein the second time period is less then about 2000 nanoseconds.

20. (Original) The processing system of claim 17, wherein the first and second voltage pump circuits generate a word line voltage of approximately five volts from a voltage supply of approximately three volts.

21. (Original) The processing system of claim 17, wherein the first voltage pump includes a first power supply connection, and wherein the second voltage pump includes a second power supply connection.

22. (Original) The processing system of claim 21, wherein the first power supply connection and the second power supply connection are each adapted to receive a power supply voltage.

23. (Original) The processing system of claim 22, wherein the first voltage pump is adapted to generate a first voltage greater than the power supply voltage.

24. (Original) The processing system of claim 22, wherein the second voltage pump is adapted to generate a second voltage greater than the power supply voltage.

25. (Original) The processing system of claim 17, wherein the first voltage pump includes a deep power down mode that is not fully powered down.

26. (Original) The processing system of claim 25, wherein the deep power down mode is controlled by a reset/power-down signal.

27. (Original) The processing system of claim 17, wherein the second voltage pump includes a deep power down mode that is not fully powered down.

28. (Original) The processing system of claim 27, wherein the deep power down mode is controlled by a reset/power-down signal.

29. (Original) The processing system of claim 17, wherein the second voltage pump is smaller than the first voltage pump.

30. (Original) The processing system of claim 17, wherein data stored in the boot block can be provided on an output data connection within approximately 300 ns following activation of the flash memory device.

31. (Original) The processing system of claim 17, wherein data stored in the additional addressable block can be provided on the output data connection after the data stored in the boot block, and within approximately 2000 ns following activation of the flash memory device.

32. (Original) A flash memory device comprising:

an array of addressable memory cells arranged in addressable blocks, the addressable blocks comprise a first memory cell location and a second memory cell location;

a first address decoder circuit coupled to the first memory cell location; and

a second address decoder circuit coupled to the second memory cell location, such that the first and second memory cell locations have two different access times from activation of the flash memory device.

33. (Original) The flash memory device of claim 32, wherein a first voltage pump circuit provides a word line voltage to the first address decoder circuit within a first time period, and a second voltage pump circuit provides a word line voltage to the second address decoder circuit within a second time period which is greater than the first time period.

34. (Original) The flash memory device of claim 33, wherein the first time period is less than about 300 nanoseconds.

35. (Original) The flash memory device of claim 33, wherein the second time period is less than about 2000 nanoseconds.

36. (Original) The flash memory device of claim 32, wherein the first and second voltage pump circuits generate a word line voltage of approximately five volts from a voltage supply of approximately three volts.

37. (Original) The flash memory device of claim 32, wherein the first voltage pump includes a first power supply connection adapted to receive a power supply voltage and a first deep power down mode that is not fully powered down, the first voltage pump being adapted to generate a first voltage greater than the supply voltage;

wherein the second voltage pump includes a second power supply connection adapted to receive a power supply voltage and a second deep power down mode that is not fully powered down, the second voltage pump being adapted to generate a second voltage greater than the supply voltage; and

wherein the first deep power down mode and the second deep power down mode are controlled by a reset/power-down signal.